

Introduction

The 40 / 100 Gigabit Ethernet MAC Core is designed to comply with the IEEE802.3ba Specification Draft 1.0. The Core can be used in either NIC (Network Interface Card) or Ethernet Switching applications. A set of configuration registers is available to dynamically set the Core to terminate and form MAC frames (NIC application) or to pass MAC frames without modification to the User application or to the Ethernet line (Switching application). When used in NIC or Switching applications, the Core provides support for IEEE managed objects, IETF MIB-II and RMON for management applications (e.g. SNMP).

On the application side, the 40 / 100 Gigabit Ethernet MAC Core implements a flexible FIFO interface that can be connected to a custom user application.

On the Ethernet line side, the Core implements either a XLGMII (40 Gigabit Medium Independent Interface) or a CGMII (100 Gigabit Medium Independent Interface), depending on the configuration of the Core.

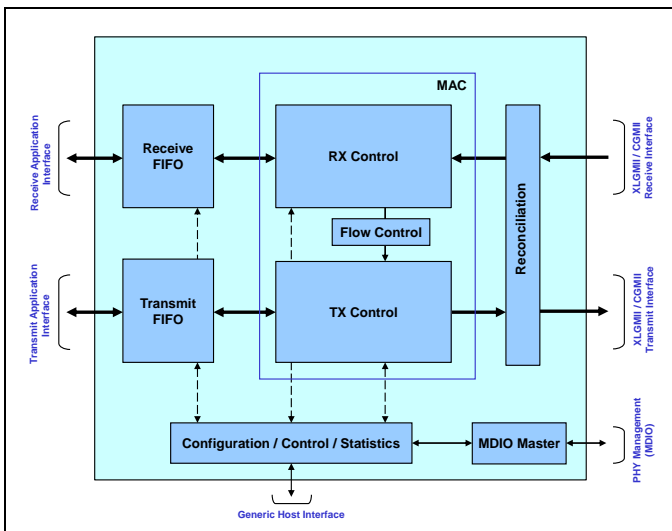
The Core implements advanced system level features like a Time Stamping Unit (TSU) and a per-channel or class based flow control mechanism.

MorethanIP also provides the 40/100GBase-R PCS Cores that can be used, in conjunction with the 40 / 100 Gigabit Ethernet MAC, to implement a 4 x 40-Bit (40 Gigabit) or 10 x 40-Bit (100 Gigabit) line interface.

The core is delivered in generic VHDL or Verilog synthesizable HDL code.

40 / 100 Gigabit Ethernet MAC Core Features Overview

- Full MAC layer and Reconciliation sub-layer implementation compliant with IEEE802.3ba Specification Draft 1.1
- Can be dynamically configured for NIC (Network Interface Card) applications or Switching / Bridging applications
- 384-Bit Transmit and Receive data-path operating at a 260.4MHz for 100Gbps operation
- Can be configured for 40 Gigabit or 100 Gigabit application
- Standard preamble and SFD (Start of Frame delimiter) insertion and deletion with optional insertion of a user specific 8-Byte preamble
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- Includes and Optional Time Stamping Unit (TSU) for IEEE1588 Applications or Other Timing Protocols
- Implements Per-Class Flow Control in Additional to the Standard Link Level Flow Control
- Optional MAC address comparison on receive and overwrite on transmit for NIC applications with programmable promiscuous mode operation
- Optional Multicast address filtering with 64-bin hash code lookup table on receive reducing processing load on higher layers
- Optional Ethernet Pause Frame (802.3 Annex 31A) termination providing fully automated flow control without any user application overhead
- Optional automatic Pause Frame generation from programmable FIFO congestion thresholds or by dedicated command pin with programmable Quanta
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG
- Clock and data rate decoupling with optional programmable asynchronous FIFOs
- Optional RAM Based statistics 32-Bit or 64-Bit counters for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)



40 / 100 Gigabit Ethernet MAC Core Block Diagram

Implementation Summary

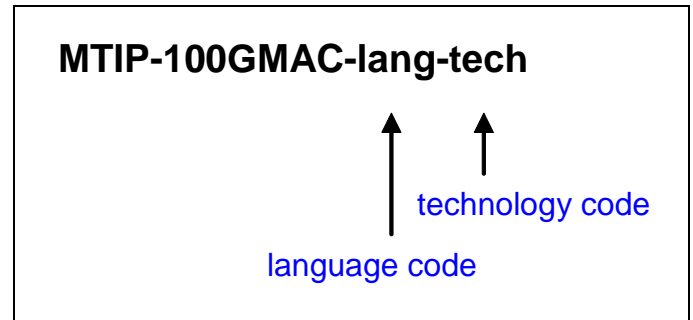
Altera FPGA Implementation Summary

Core Specifics		
Supported Device Family	Stratix IV GT / ASICs	
Resources Used		
	Min	Max
ALUTs	18,000	22,000
Registers	18,500	20,000
RAM	0 (No FIFO Back-end)	~50K bits
Supported Design Tools		
Altera Tool	Quartus II 9.0 or Later	
Synthesis	Quartus II 9.0 or Later	
Speed Grade		
-C2 (40Geth and 100Geth Operation)		
-C4 (40Geth Operation Only)		

Deliverables

- Verilog / VHDL Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Self Checking Verilog or VHDL testbenches and Verification test cases
- Comprehensive Documentation, Datasheet and User Guide
- Industry-standard Synopsys Design Constraints (SDC) File for Synthesis and Timing Analysis
- Support Directly by MorethanIP Expert Developers

Ordering Code



Language Code	Delivery Language
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Altera FPGA technology.

Technology Code	Target Technology
GEN	Generic synthesizable code for ASIC or FPGA implementations.
ALTR	Synthesizable code optimized for Altera FPGAs.

Contact

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