

Introduction

The 40/100 Gigabit Ethernet MAC Core is designed to comply with the IEEE802.3ba Specification. The Core can be used in either NIC (Network Interface Card) or Ethernet Switching applications. A set of configuration registers is available to dynamically set the Core to terminate and form MAC frames (NIC application) or to pass MAC frames without modification to the User application or to the Ethernet line (Switching application). When used in NIC or Switching applications, the Core provides support for IEEE managed objects, IETF MIB-II and RMON for management applications (e.g. SNMP).

On the application side, the MAC Core implements a flexible FIFO interface that can be connected to a custom user application.

On the Ethernet line side, the Core implements a 192bit XL/CGMII (40/100 Gigabit Medium Independent Interface).

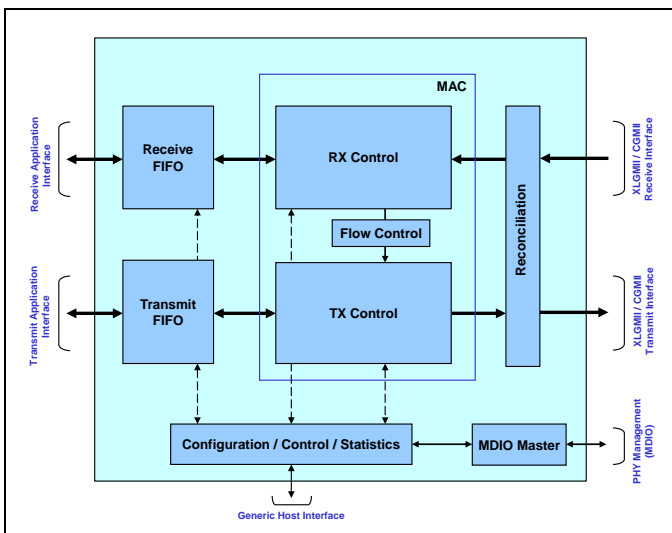
The Core implements advanced system level features like a Time Stamping Unit (TSU) and a priority or class based flow control mechanism (PFC Pause Frame).

MorethanIP also provides the 40GBase-R and 100GBase-R PCS Cores that can be used, in conjunction with the MAC Core, to implement the line interface.

The core is delivered in generic VHDL or Verilog synthesizable HDL code.

40/100G Ethernet MAC Core Features Overview

- Full MAC layer and Reconciliation sub-layer implementation compliant with IEEE802.3ba Specification Draft
- Can be dynamically configured for NIC (Network Interface Card) applications or Switching / Bridging applications
- 256-Bit Transmit and Receive Application Interface
- 192-Bit Line Interface operating at 261MHz for 40Gbps operation and 651MHz for 100G operation
- Standard preamble and SFD (Start of Frame delimiter) insertion and deletion with optional insertion of a user specific preamble
- Lane, data alignment, PHY error and local/remote fault signaling handled by the Core's Reconciliation sub-layer
- Includes and Optional Time Stamping Unit (TSU) for IEEE1588 Applications or other Timing Protocols
- Implements Per-Class Flow Control in addition to the Standard Link Level Flow Control (Pause Frame)
- Optional MAC address comparison on receive and overwrite on transmit for NIC applications with programmable promiscuous mode operation
- Optional Multicast address filtering with 64-bin hash code lookup table on receive reducing processing load on higher layers
- Optional Ethernet Pause Frame (802.3 Annex 31A) termination providing fully automated flow control without any user application overhead
- Optional automatic Pause Frame generation from programmable FIFO congestion thresholds or by dedicated command pin with programmable Quanta
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG
- Clock and data rate decoupling with optional programmable asynchronous FIFOs
- Optional statistics 32-Bit or 64-Bit counters for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)



40/100 Gigabit Ethernet MAC Core Block Diagram

Implementation Summary

Core Specifics		
Supported Device Family	Stratix IV GT (40G only)/ ASIC (40G/100G)	
Resources Used		
	Min	Max
ALUTs (FPGA)	24,000	
Registers	20,000	
RAM	~70K bits (FIFO Backend)	
Supported Design Tools		
Altera Tool	Quartus II 9.0 or Later	
Synthesis	Quartus II 9.0 or Later Synopsys DC (any)	
Speed Grade (FPGA)		
-C2/C3 (40G only)		

Deliverables

- Verilog / VHDL Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Self Checking Verilog or VHDL testbenches and Verification test cases
- Documentation: Datasheet and User Guide
- Synthesis Example Scripts
- Industry-standard Synopsys Design Constraints (SDC) File for Synthesis and Timing Analysis
- Support Directly by MorethanIP Expert Developers

Ordering Code

MTIP-CGMAC192-lang-tech

Language Code	Delivery Language
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Altera FPGA technology.

Technology Code	Target Technology
GEN	Generic synthesizable code for ASIC or FPGA implementations.
ALTR	Synthesizable code optimized for Altera FPGAs.

Contact

MorethanIP

E-Mail : info@morethanip.com
 Internet : www.morethanip.com

Muenchner Strasse 199
 D-85757 Karlsfeld
 Germany

Tel : +49 (0) 8131 333939 0
 FAX : +49 (0) 8131 333939 1