

Introduction

The RXAUI (10 Gigabit Reduced Attachment Unit Interface) interface provides a low pin count board level interface to connect a 10 Gigabit Ethernet MAC to a physical device or for backplane connectivity.

The RXAUI PCS Core implements a XGXS (10 Gigabit Extension Sub-Layer) PCS function (Physical Coding Sub-Layer) Core, designed to comply with the IEEE802.3ae Clause 48 and can be used, with four to two multiplexing and two to four lane demultiplexing functions.

The RXAUI Core provides a low pin count board level interface to PHY devices or for backplane applications. The Core is also compliant for Dune Network Dual Rate PHY interface.

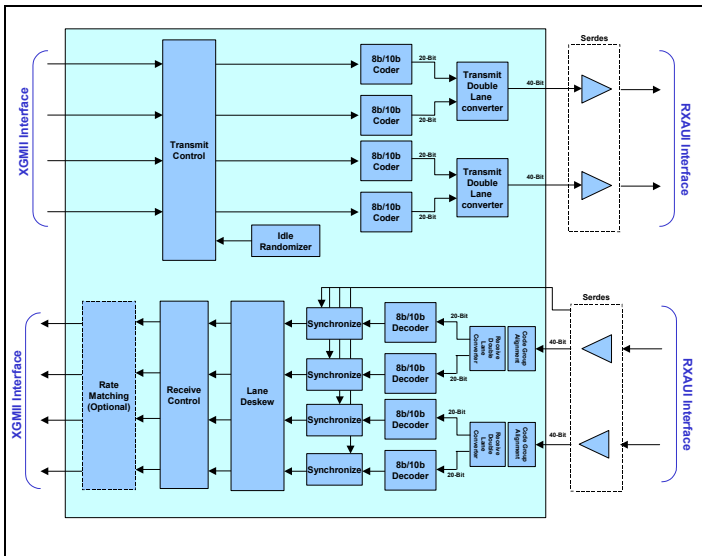
On the MAC or application side, the RXAUI PCS Core implements a 64-Bit de-multiplexed XGMII interface or a standard 32-Bit DDR (Dual Data Rate).

On the line side can be used in combination with an embedded Dual 6.25Gbps SERDES or, via a dual 20-Bit interface, with an external SERDES.

The Core can be used with Xilinx Virtex 5FXT parts to increase per device port density and improve board level design.

RXAUI PCS Core Features Overview

- Implements a XGXS PCS function fully compliant with the IEEE802.3ae Clause 48 specification
- Core XGXS functions passed complete UNH certification
- Implements XGXS PCS frame encapsulation / de-encapsulation with Start, Terminate ordered set insertion / termination and Randomized Idle ordered set generation during inter-packet gap
- Implements receive link synchronization state machine and 10-Bit data alignment from SERDES with Comma character detection
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Dual 20-Bit interface to embedded or external 6.25Gbps SERDES
- Implements a 64-Bit XGMII interfaces that can be seamlessly connected to MorethanIP 10 Gigabit Ethernet MAC Core or to any other third party MAC Core
- Optional rate matching to adapt Rates from the RXAUI Line clock with the XGMII Receive Clock
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Implements a link synchronization state machine per port
- Receive Lane alignment (Deskew) designed to compensate RXAUI lines skew
- Line alignment exceeds IEEE802 lane skew tolerance requirements
- Rate matching
- The RXAUI Core can be implemented in Xilinx Virtex 5FXT FPGAs, Structured ASICs or ASICs.
- The Core is optionally be delivered in Verilog source code or encrypted Verilog code which provides a lower cost licensing option



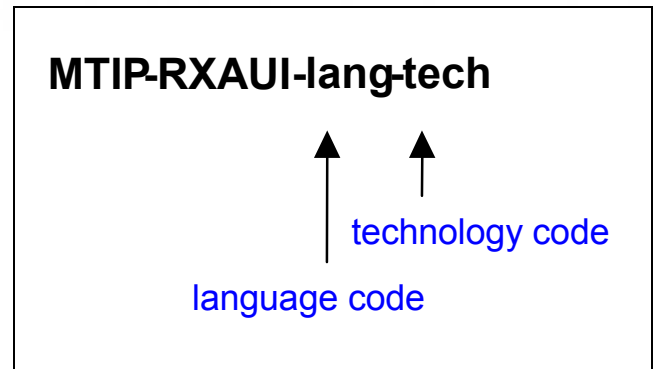
10 Gigabit Ethernet RXAUI Core Block Diagram

Implementation Summary

Xilinx FPGA Implementation Summary

Core Specifics		
Supported Device Family	Virtex-5 FXT	
Version	1.0	
Resources Used		
	Without Rate Matching	With Rate Matching
LUTs	2745	3022
FFs	2318	2565
Block RAM	0	2
GTP	1	1
Provided with Core		
Documentation	Datasheet, User Guide	
Design File Formats	Source RTL Verilog Encrypted RTL Verilog	
Constraints File	UCF File	
Verification	Verilog Self-Checking Testbench	
Supported Design Tools		
Xilinx Tool	10.1i or Later	
Simulation	Modelsim 6.2g or Later	
Synthesis	XST	
Required Speed Grade		
-2		

Ordering Code



Language Code	Delivery Language
VHDL	Synthesizable RTL VHDL Source Code.
VLOG	Synthesizable RTL Verilog Source Code.
BIN	Encrypted RTL for Xilinx FPGA technology.

Technology Code	Target Technology
GEN	Generic synthesizable code for ASIC or FPGA implementations
XLNX	Synthesizable code optimized Xilinx FPGAs.

Contact

MorethanIP

E-Mail : info@morethanip.com

Internet : www.morethanip.com

Muenchner Strasse 199

D-85757 Karlsfeld

Germany

Tel : +49 (0) 8131 333939 0

FAX : +49 (0) 8131 333939 1