

Introduction

With the deployment of Fast Ethernet to the desktop, Gigabit Ethernet has become the standard backbone link to connect workgroup switches to backbone switches or access routers.

The IEEE802.3-2002 specification defines, in Clause 36, a family of Physical Coding Sublayers (PCS) collectively known as 1000Base-X. It covers three embodiments within this family:

- 1000Base-CX for two pairs balanced copper cabling
- 1000Base-LX for long wavelength optical transmission
- 1000Base-SX for short wavelength optical transmission

In addition to standard compliance, the Core provides support for proprietary or industry standard 2500Base-X 2.5Gbps, 2000Base-X 2Gbps Ethernet connections.

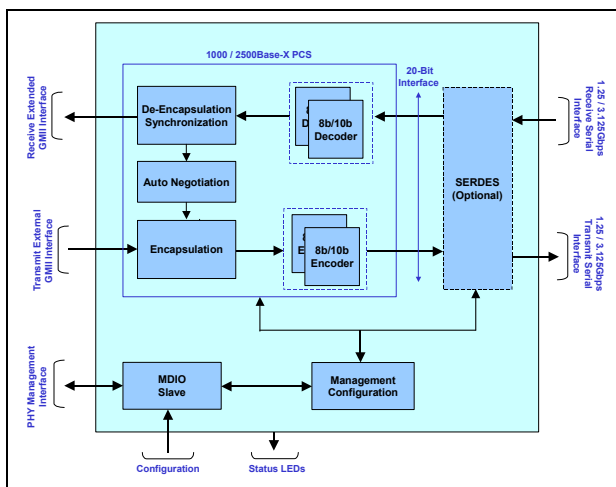
The Core is compliant with Clause 36 of the IEEE802.3 standard and implements 8B/10B coding, link synchronization, frame encapsulation generation / termination. The Core also supports Auto-Negotiation (Clause 37 of IEEE802.3 standard).

The core can seamlessly connect to any industry standard Gigabit Ethernet SERDES (SERializer / DESerializer) device via a 20-Bit SDR or 10-Bit DDR interface and to the MorethanIP AnySpeed MAC Layer device with a 16-Bit Extended GMII (Gigabit Media Independent Interface).

The Core implements a PHY Management interface (MDIO) with control and management registers as defined in Clause 45 of the IEEE 802.3 specification.

1000 / 2500Base-X PCS core Features

- Implements Clause 36 of 802.3-2002 specification for 1000Base-X family of PCS (Physical Coding Sub-layer)
- Supports industry standard 2500Base-X / 2000Base-X connections or any Ethernet speeds up to 2.5Gbps
- Implements a 20-Bit Serdes interface and optionally, a 10-Bit DDR (Dual Data Rate) Serdes interface
- Extended 16-Bit GMII interface compatible with MorethanIP AnySpeed MAC Core
- Implements PCS frame encapsulation / de-encapsulation with /S/, /T/ orderset insertion / termination and // Idle ordered set generation during inter-packet gap
- Implements receive link synchronization state machine and 10-Bit data alignment from SERDES with K28.5 character detection
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Implements User controllable 1000Base-X Auto-Negotiation (IEEE 802.3 Clause 37) which fully programmable node ability register
- Dual Gigabit / 2.5Gbps implementation with Embedded Stratix-II GX Serdes or discrete Serdes solution
- MDIO Slave PHY Management interface which provides a standard interface for Core configuration and management
- Implements standard management register set as defined in Clause 45 of IEEE802.3 which specific Extended registers for improved flexibility
- Programmable physical MDIO address via an external 5-Bit address
- Programmable (Via PHY Management interface) GMII Loopback
- Can be implemented in Altera FPGAs or ASICs
- Can optionally be delivered in VHDL or Verilog source code or netlist which provides a lower cost licensing option



1000 / 2500Base-X PCS Core Block Diagram

Implementation Summary

Altera FPGA Implementation Summary

| Target Device Family | Speed Grade | Complexity | Performance |
|----------------------|-------------|-------------|-------------|
| Stratix II | C5 | 840 LEs (1) | 178MHz |
| Stratix II GX | C5 | 463 LEs (1) | 178MHz |

1. The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

| Target Device Family | Complexity | Performance |
|----------------------|-------------|-------------|
| Hardcopy II | 3900 HCells | 210Mhz |

Deliverables

- Verilog / VHDL Synthesizable RTL HDL or encrypted RTL for FPGA implementation
- Behavioral Verilog or VHDL testbenches and Verification test cases
- Support for FPGA and ASIC design tools

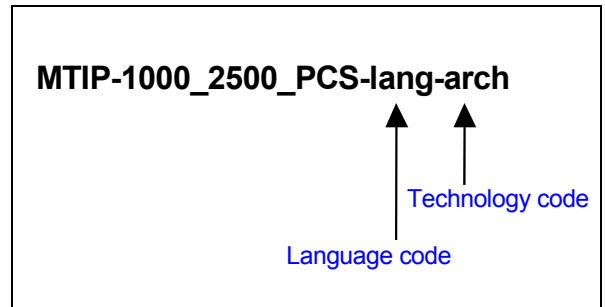
Development Boards

- Standard Stratix II GX FPGA Prototyping / Development Boards



Prototyping / Development Board

Ordering Code



Language Code

| Language Code | Delivery Language |
|---------------|--------------------------------------------------------------------------------------------------------|
| BIN | Encrypted VHDL / Verilog Sources Code for Altera FPGAs and Structured ASICs. |
| VHDL | Synthesizable generic VHDL source code for Altera FPGA and Structured ASICs or ASICs implementations |
| VLOG | Synthesizable generic Verilog source code for Altera FPGA and Structured ASICs or ASIC implementations |

Technology Code

| Technology Code | Technology |
|-----------------|---------------------------------------------------------------|
| GEN | Source code option for FPGA, Structured ASICs and ASICs. |
| ALTR | Encrypted RTL for Altera FPGAs and Hardcopy Structured ASICs. |

Contact

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