

1 Introduction

The MAC-NET Core implements, in conjunction with a triple speed 10/100/1000 MAC, Layer 3 network acceleration functions, which are designed to accelerate the processing of various common networking protocols such as IP, TCP, UDP and ICMP providing wire speed services to Client applications.

The Core implements a triple speed 10/100/1000Mbps Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with Full Duplex Gigabit Ethernet LANs and legacy Half or Full Duplex 10/100Mbps Ethernet and Fast Ethernet LANs.

The MAC operation is fully programmable and can be used in NIC (Network Interface Card), bridging or switching applications. For SNMP (Simple Network Management Protocol) the Controller implements Management Information Base (MIB, MIB-II) according to IETF RFC2665 and Remote Network Monitoring (RMON) according to IETF RFC 2819. All registers are accessible via a 32-Bit parallel interface.

The Core also implements a Hardware acceleration block to optimize the performance of network controllers providing IP and TCP,UDP,ICMP protocol services. The acceleration block performs, in hardware, critical functions, which are typically implemented with large software overhead.

The Core implements programmable embedded FIFOs that can provide, on the Receive path, buffering for loss-less flow control

Advanced Power Management features are available with Magic Packet detection and programmable power down modes.

The Core provides a flexible and evolutive solution for a large number of applications such as SAN (Storage Area Network), NAS (Network Attached Storage), Enterprise File Servers, Firewalls, Gateways or Routers.

The MAC-NET Core can be implemented in FPGA or ASIC.

2 Block Diagram

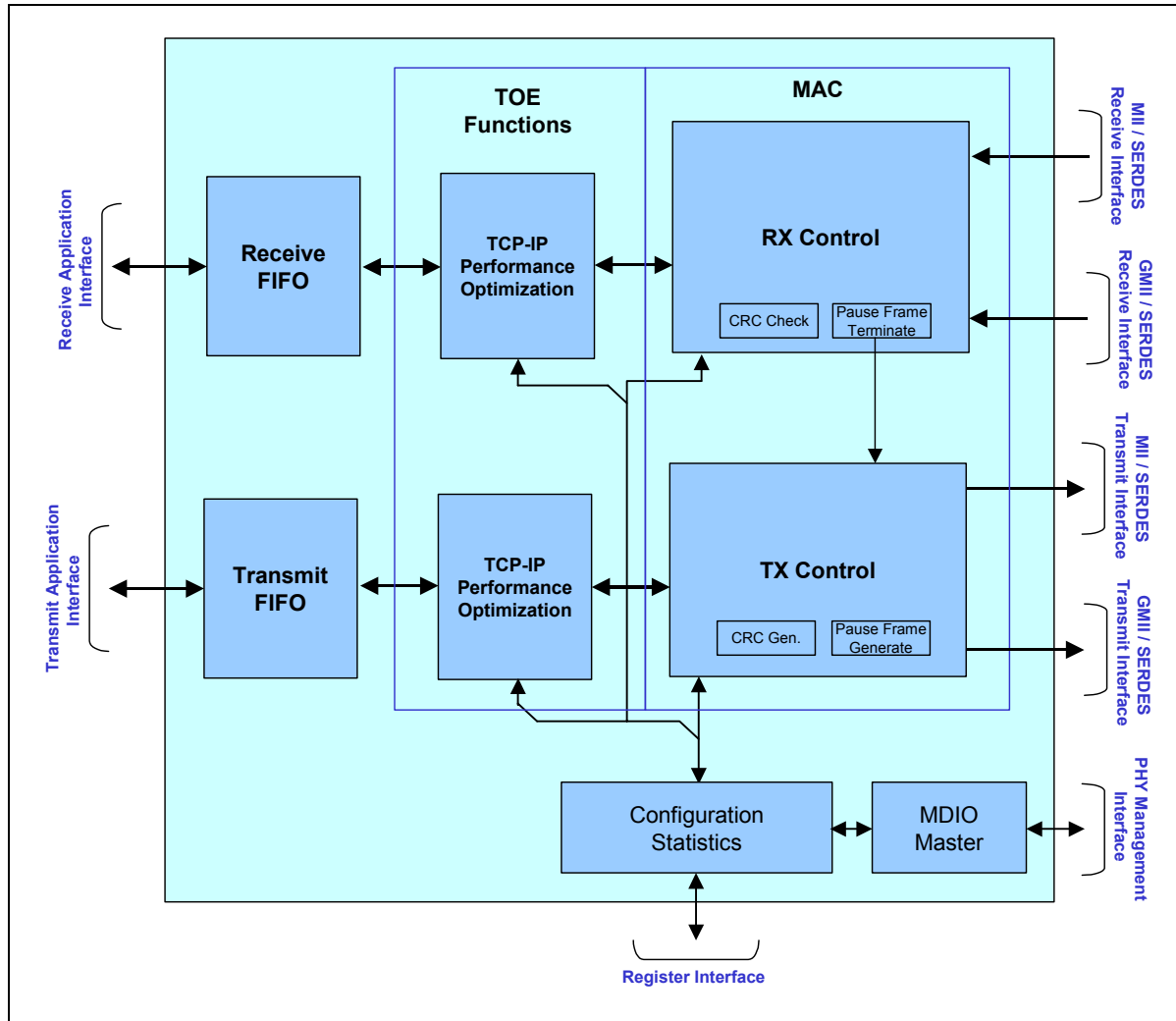


Figure 1: 10/100/1000 Ethernet MAC with Protocol Acceleration Functions Block Diagram

3 10/100/1000 Ethernet MAC-NET Core Key Features

Ethernet MAC Features

- Implements the full 802.3 specification with preamble / SFD generation, frame padding generation, CRC generation and checking
- Dynamically configurable to support 10Mbps, 100Mbps or 1Gbps operation
- Supports full duplex operation
- Supports AMD Magic Packet detection with interrupt for node remote power management
- Seamless interface to commercial Gigabit Ethernet PHY device via a 8-Bit Gigabit Medium Independent Interface (GMII) operating at 125MHz
- Seamless interface to commercial Fast Ethernet PHY device via a 4-Bit Medium Independent Interface (MII) operating at 25MHz
- 32-bit asynchronous FIFO Interface with programmable threshold settings
- CRC-32 checking at full speed with optional forwarding of the FCS field to client
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- Implements fully automated Pause Frame (802.3 Annex 31A) generation and termination providing flow control without user application intervention
- Pause quanta used to form Pause frames, dynamically programmable
- Pause frame generation additionally controllable by user application offering flexible traffic flow control
- Optional forwarding of received pause frames to the user application
- Implements standard flow-control mechanism in full-duplex operation mode
- Support for VLAN tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames)
- Programmable group of four supplemental MAC addresses that can be used to filter Unicast traffic
- Programmable Promiscuous mode support to omit MAC destination address checking on receive
- Multicast address filtering on receive based on 64 entries hash table reducing higher layer processing load
- Programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames)
- Statistics indicators for frame traffic as well as errors (alignment, CRC, length) and pause frames providing for IEEE 802.3 basic and mandatory Management Information Database (MIB) package as well as Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)
- Separate status word available for each received frame on the user interface providing information such as frame length, frame type, VLAN tag and error information

- MDIO Master interface for PHY device configuration and management with two programmable MDIO base addresses
- Available for CPLD or ASIC implementation as well as an ASSP (application specific standard part)
- Design Kit comes with extensive Ethernet frame generators and checking models enabling fully automated design verification and testing for standard compliance and error behavior, enabling for fast turn-around design cycles

IP Protocol Acceleration Features

- Operates on TCP/IP and UDP/IP and ICMP/IP protocol data or IP header only
- Enables wire-speed processing up to Gigabit Ethernet
- Transparent passing of frames of other types and protocols
- Support for VLAN tagged frames according to IEEE 802.1q with transparent forwarding of VLAN tag and control field
- Automatic IP-header and payload (protocol specific) checksum calculation and verification on receive
- Automatic IP-header and payload (protocol specific) checksum generation and automatic insertion on transmit configurable on a per-frame basis
- Support for IP and TCP, UDP, ICMP data for checksum generation and checking
- Full header options support for IPv4 and TCP protocol headers
- IPv6 support limited to datagrams with base header only. Datagrams with extension headers are passed transparently unmodified/unchecked.
- Statistics information for received IP and protocol errors
- Configurable automatic discard of erroneous frames
- Configurable automatic Host-to-Network (RX) and Network-to-Host (TX) byte order conversion for IP and TCP/UDP/ICMP headers within the frame
- Configurable padding remove for short IP datagrams on receive
- Configurable Ethernet IPv4 and IPv6 Type removal on receive and automatic insertion on transmit to allow for 32-bit word aligned header and payload processing
- Store&Forward operation with clock and rate decoupling FIFOs

4 Implementation Summary

Table 1: 10/100/1000 Ethernet MAC-NET Complexity Summary

Target Device Family	Speed Grade	Complexity (With 2048 Byte FIFO per direction)		Performance	MAC Requirement (Ethernet Speed)
		LEs	RAM bits		
STRATIX	-7	4820	48032	133 MHz	125MHz (Gigabit)
CYCLONE	-7	4820	48032	132 MHz	125MHz (Gigabit)
STRATIX-II	-5	4340 (ALUT)	48032	160 MHz	125MHz (Gigabit)
CYCLONE-II	-7	4850	48032	133 MHz	125MHz (Gigabit)

5 Design Kit Overview

Table 2: Design Kit Overview

<i>Design and Simulation</i>	
Language	Optimized VHDL / Verilog or lower cost FPGA encrypted netlist.
Simulation	Configurable VHDL / Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive test environment with Ethernet frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
<i>Supported Design Tools</i>	
Simulation	Modelsim Version 5.7a or higher.
Synthesis	Exemplar 2003a or higher Exemplar Precision 2003c or higher Synplicity Synplify 7.3 or Higher Quartus II 4.1 or higher
Implementation	Quartus II 4.1 or higher

6 Ordering Code

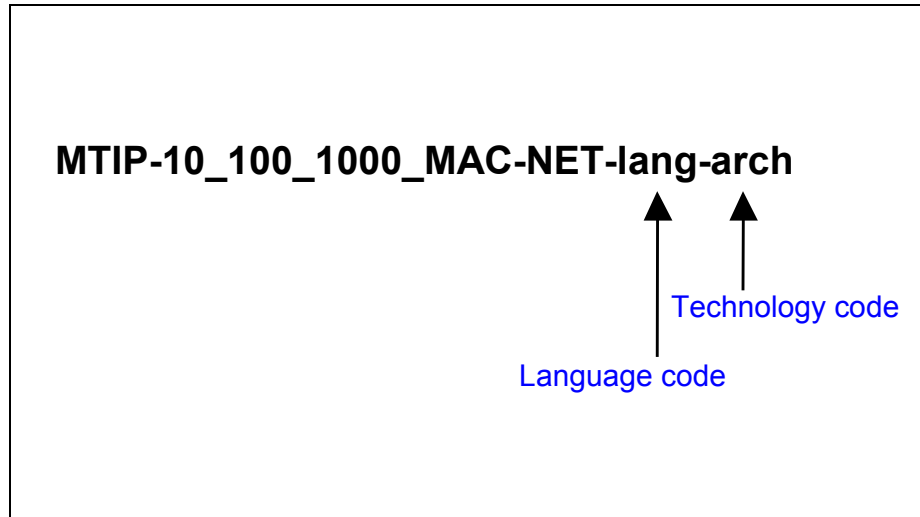


Table 3: Language Code

Technology Code	Target Technology
BIN	Encrypted FPGA netlist.
VHDL	Synthesizable generic VHDL source code for FPGA or ASIC implementations
VLOG	Synthesizable generic Verilog source code for FPGA or ASIC implementations

Table 4: Technology Code

Technology Code	Target Technology
GEN	Source code option for Altera FPGAs or ASIC implementations.
ALTR	Encrypted netlist for Altera FPGAs.

7 References

- IEEE 802.3 2002 Edition
- IEEE 802.1Q 1998 Edition
- RFC2665, Definitions of Managed Objects for the Ethernet-like Interface Type
- RFC2863, The interfaces Group MIB
- IETF RFC 791, Internet Protocol (IPv4)
- IETF RFC 792, Internet Control Message Protocol (ICMP)
- IETF RFC 793, Transmission Control Protocol (TCP)
- IETF RFC 768, User Datagram Protocol (UDP)
- IETF RFC 894, Transmission of IP Datagrams over Ethernet Networks
- IETF RFC 2460, Internet Protocol, Version 6 (IPv6)
- IETF RFC 2464, Transmission of IPv6 Packets over Ethernet Networks

8 Contact

MorethanIP GmbH

An der Steinernen Brücke 1

85757 Karlsfeld, Germany

Tel : +49 (0) 81313339390

FAX : +49 (0) 81313339391

E-Mail : info@morethanip.com

Internet : www.morethanip.com