

1 Introduction

An Ethernet switch is used to interconnect a number of Ethernet LANs (Local Area Networks), forming a large Ethernet network. Different ports of the switch are connected to different LAN segments. The purpose of the switch is to forward the packets intelligently, only to the desired destination segment of the network whenever possible, instead of flooding the network for every frame. The switch stores the MAC addresses observed from frames received through each port and uses this information to learn which MAC belongs to which segment of the network. With this information, the switch can forward the frames from the source network segment to only the destination, instead of forwarding the frame to all the connected ports, reducing the network load.

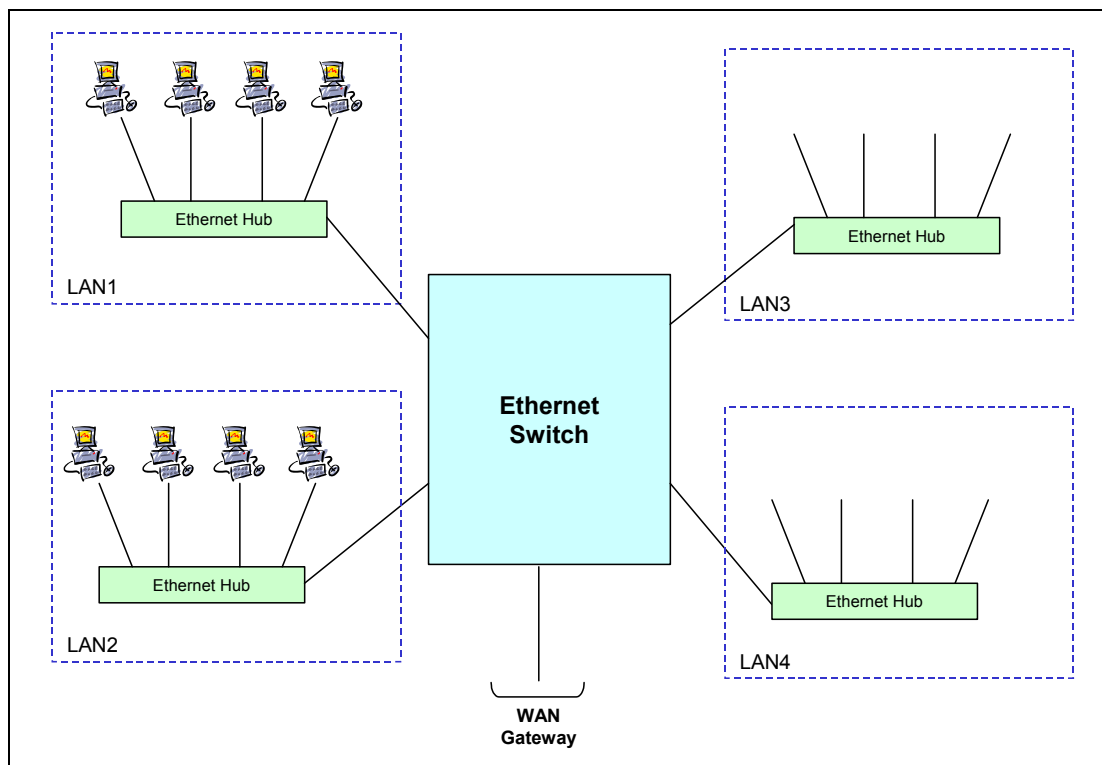


Figure 1: Switched LAN Example

While standard Ethernet multi-port Ethernet Switches can be used to meet a number of applications, MorethanIP programmable switch platform can be configured to provide more flexibility. For example, standard Ethernet Switches typically only implement physical Ethernet interfaces such as MII (Fast Ethernet ports) or GMII (Gigabit Ethernet port) and therefore require an adaptation device (e.g. FPGA, ASIC) if one port needs to be connected to, for example, a PCI bus, a SONET / SDH framer for POS (Packet Over SONET / SDH) or EOS (Ethernet Over SONET / SDH) applications or voice processors for VoIP (Voice over IP) applications.

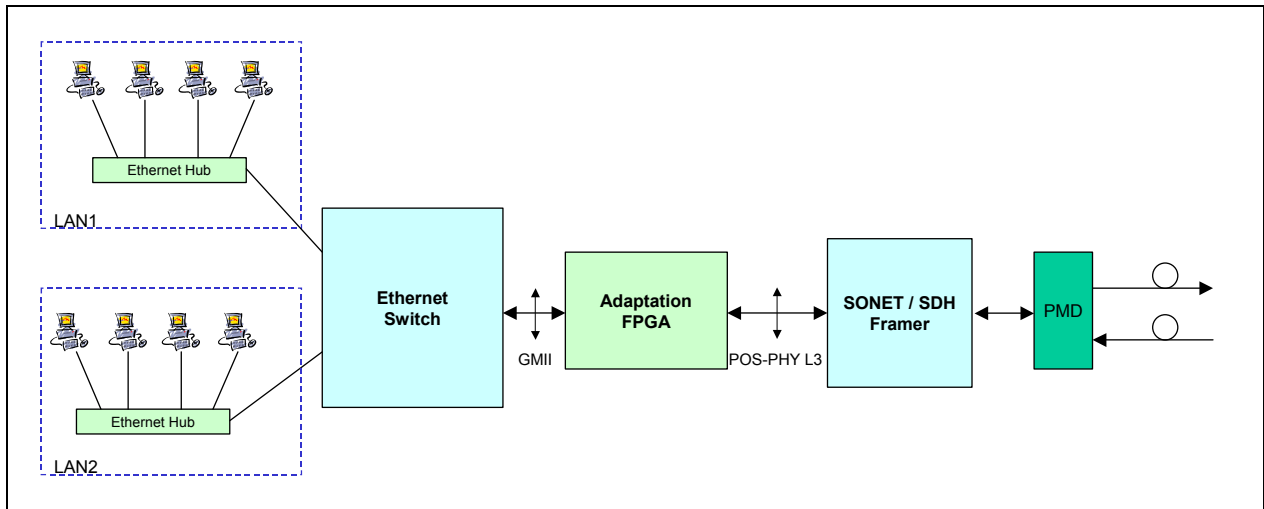


Figure 2: POS Application Example

The MorethanIP Ethernet switching solution provides a flexible and unique solution allowing designers to implement any additional function (e.g. PCI interface, POS-PHY / SPI packet interfaces,...) to complement the Ethernet switch and to provide connectivity to a large number of standard parts (e.g. SONET / SDH framers, VoIP processor) or systems (e.g. Proprietary backplane, host computer via PCI / PCI-X) with a single chip solution.

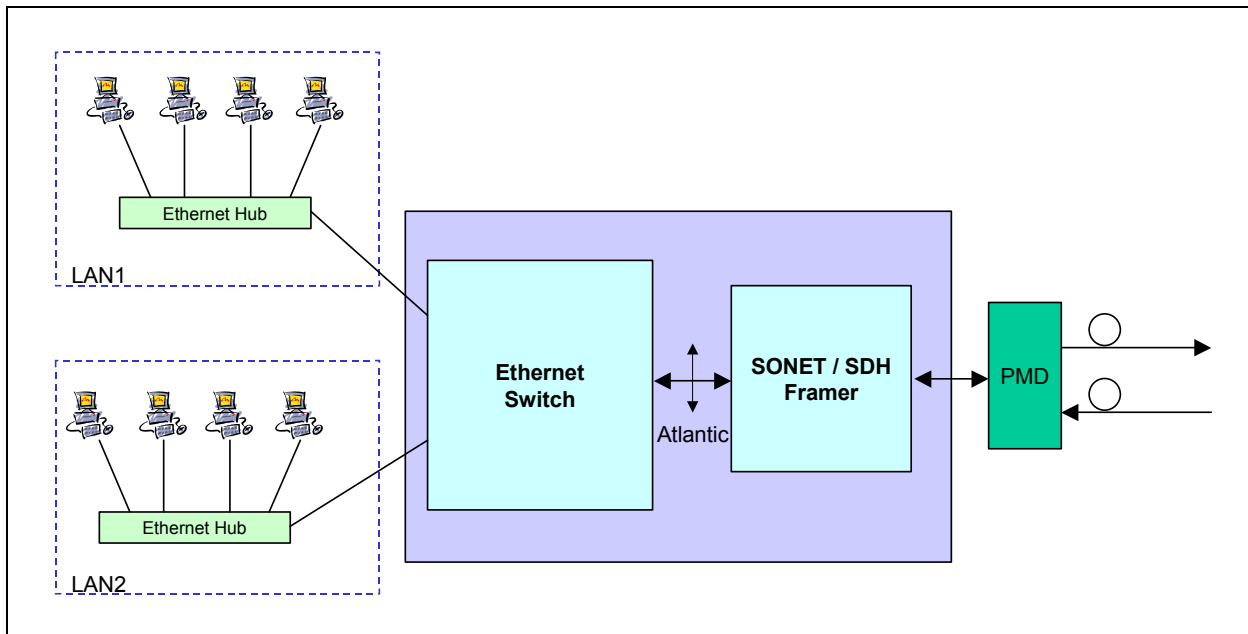


Figure 3: POS Application Example with MorethanIP Switching Solution

The MorethanIP switch implement a programmable number of Atlantic ports, which can be seamlessly connected to any Telecom Core from MorethanIP or to any third party Core supporting the Atlantic SOC (System on a Chip) standard. Each Atlantic port is 32-Bit wide.

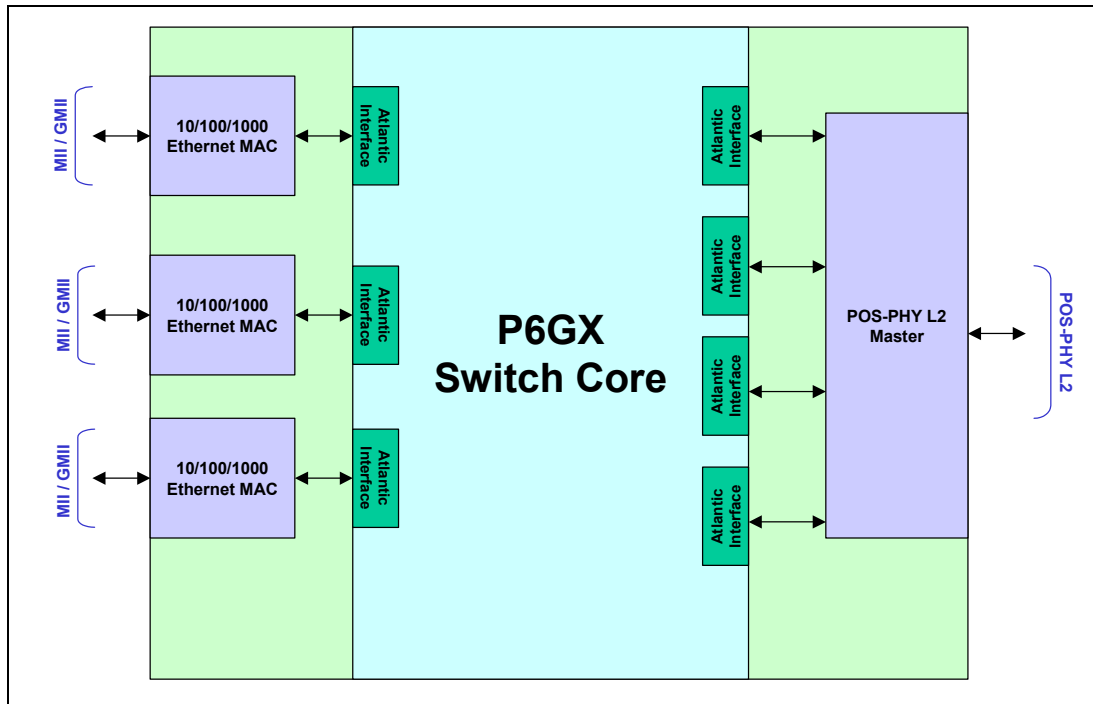


Figure 4: Integrated Switch Solution Example

In addition, standard Ethernet switches typically implement a large number of ports (12, 24) and implement a fixed distribution of ports (e.g. eight 10/100 Ethernet ports + 1 Gigabit Ethernet port) and therefore can provide an oversized or not adapted solution for applications that require only a few ports or a different repartition of ports.

The MorethanIP P6GESX programmable switch provides up 8Gbps-switching capability, which can be used as required by the User application. MorethanIP switch is implemented as a System on Chip (SOC) and it embeds a Hardware switch engine, for performance, and a 32-Bit processor, which performs learning, ageing, migration tasks and which can be programmed to implement any other high function such as Spanning Tree or any user specific task.

The MorethanIP P6GESX Core is available on Altera Stratix FPGAs (Field Programmable Gate Array), which provides a quick time-to-market. The Switch Core can be migrated to Altera Hardcopy or ASIC devices to reduce costs.

2 P6GESX 6Gbps Ethernet Switch Features

- Integrated Ethernet Switch engine with programmable number of SOC (System on Chip) ports
- 32-bit switching engine operating at frequencies up to 260MHz on Altera Stratix-II FPGA providing 8Gbps non-blocking switching capacity
- Implements hardware three-stage switching look-up mechanism providing a learning capacity of up to 2K MAC addresses
- Configurable broadcast domain resolution to forward broadcast frames or unknown destination frames to dedicated ports only instead of all
- Configurable multicast domain resolution to forward multicast frames to dedicated ports only instead of all
- Individual port enable/disable
- Configurable Mirror port which, when enabled, receives all traffic from all ports, for debug purposes
- Switching table range can be reduced, for optimized Firmware operation, to support 700 or 1K MAC addresses
- Programmable firmware operation with Static or Dynamic (learning, aging) switching tables
- Embedded NIOS 32-Bit processor with 64K-Byte internal program memory sufficient for MorethanIP standard switching firmware (Learning, Aging, Migration and look-up management) and user specific tasks
- Support Ethernet Multicast, Broadcast with flooding control to avoid unnecessary duplication of frames
- Supports VLAN frames reception and transmission
- Programmable number of IP Core interconnect Atlantic ports which can be connected to up to 16 Ethernet MACs, packet interface queues or custom logic
- Can be used in managed implementations, with an external configuration and control processor, or in unmanaged implementations with external configuration and control pins
- Event and status signals which can be used to monitor port activity, severe error conditions or any user specific event
- Available on Altera Stratix, Stratix-II FPGAs, Altera Hardcopy Structured ASIC and Generic ASIC
- Switch SDK (Software Development Kit) available to provide customer specific software development capability
- Fully Integrated in Altera SOPC Builder

3 Block Diagram

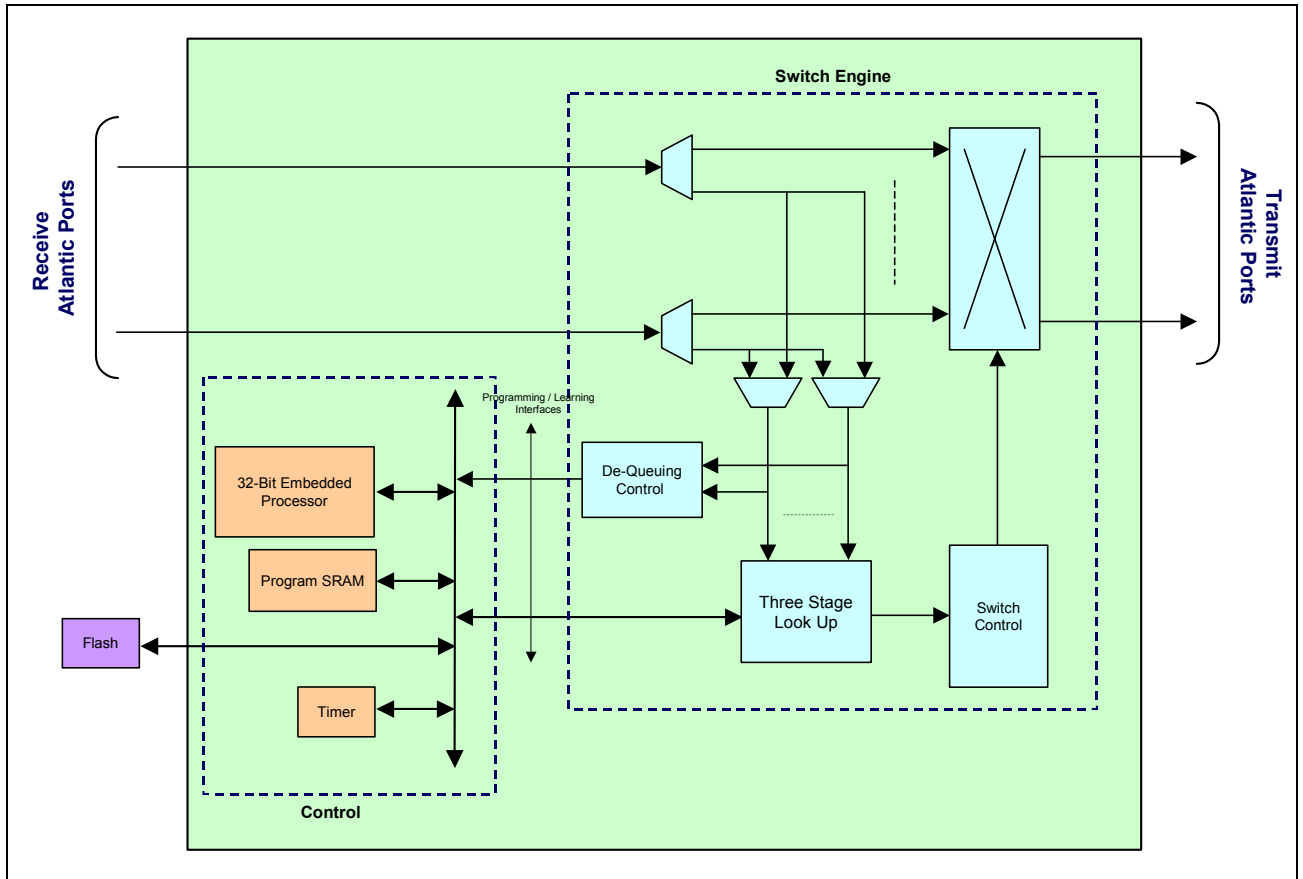


Figure 5: P6GESX L2 Switch Block Diagram

4 Implementation Summary

Table 1: P6GESX L2 Switch Complexity Summary

Device Family	Speed Grade	Complexity		Performances	
		L2 Engine	L2 Engine with Embedded NIOS Processor	Maximum Clock Frequency	Switching Capacity
STRATIX II	-5	2100 LEs ⁽¹⁾	5800 LEs ⁽¹⁾	190MHz	6Gbps
	-3			260MHz	8Gbps
STRATIX	-7	2300 LEs	6200 LEs	145MHz	4.6Gbps
	-5			200MHz	6.4Gbps

1. The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

5 10/100/1000Mbps Ethernet MAC Design Kit Overview

Table 2: Design Kit Overview

<i>Design and Simulation</i>	
Language	Source Code VHDL, Encrypted VHDL or Verilog Netlist
Simulation	Configurable VHDL / Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive test environment with Ethernet frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
<i>Supported Design Tools</i>	
Simulation	Modelsim Version 5.7a or higher.
Synthesis	Quartus II 4.1 or higher
Implementation	Quartus II 4.1 higher

6 Contact

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