

1 Introduction

An Ethernet switch is used to interconnect a number of Ethernet LANs (Local Area Networks), forming a large Ethernet network. Different ports of the switch are connected to different LAN segments. The purpose of the switch is to forward the packets intelligently, only to the desired destination segment of the network whenever possible, instead of flooding the network for every frame. The switch stores the MAC addresses observed from frames received through each port and uses this information to learn which MAC belongs to which segment of the network. With this information, the switch can forward the frames from the source network segment to only the destination, instead of forwarding the frame to all the connected ports, reducing the network load.

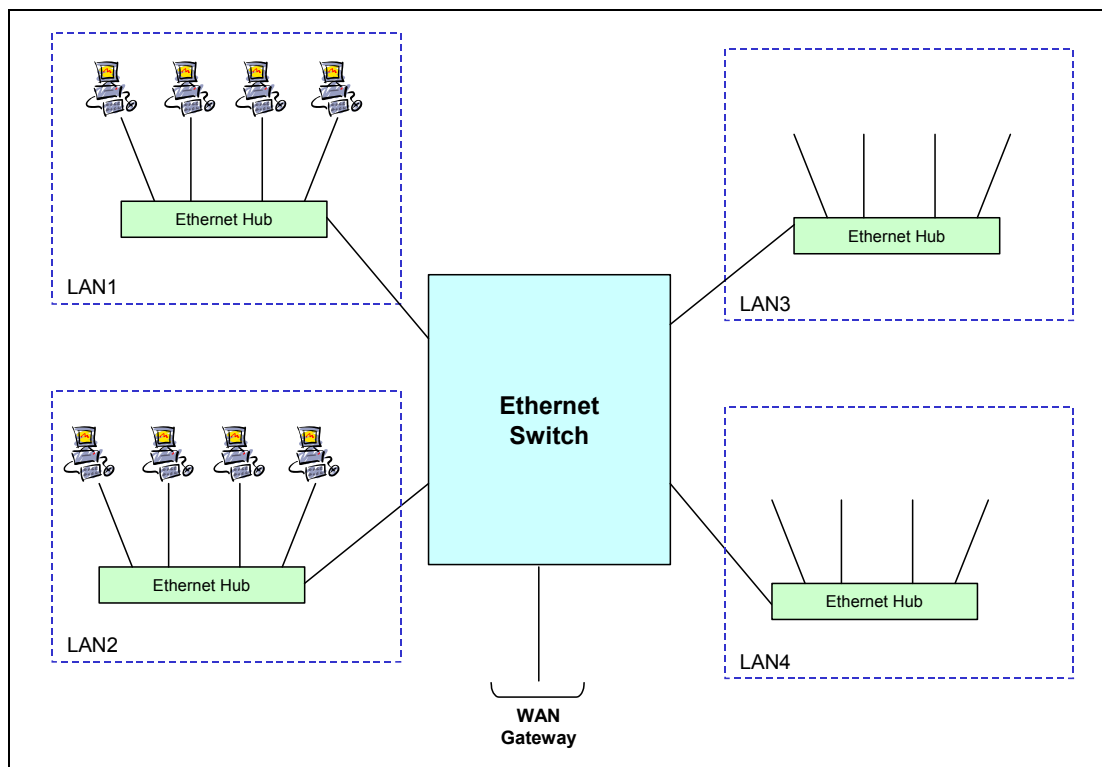


Figure 1: Switched LAN Example

While standard Ethernet multi-port Ethernet Switches can be used to meet a number of applications, MorethanIP programmable switch platform can be configured to provide more flexibility. For example, standard Ethernet Switches typically only implement physical Ethernet interfaces such as MII (Fast Ethernet ports) or GMII (Gigabit Ethernet port) and therefore require an adaptation device (e.g. FPGA, ASIC) if one port needs to be connected to, for example, a PCI bus, a SONET / SDH framer for POS (Packet Over SONET / SDH) or EOS (Ethernet Over SONET / SDH) applications or voice processors for VoIP (Voice over IP) applications.

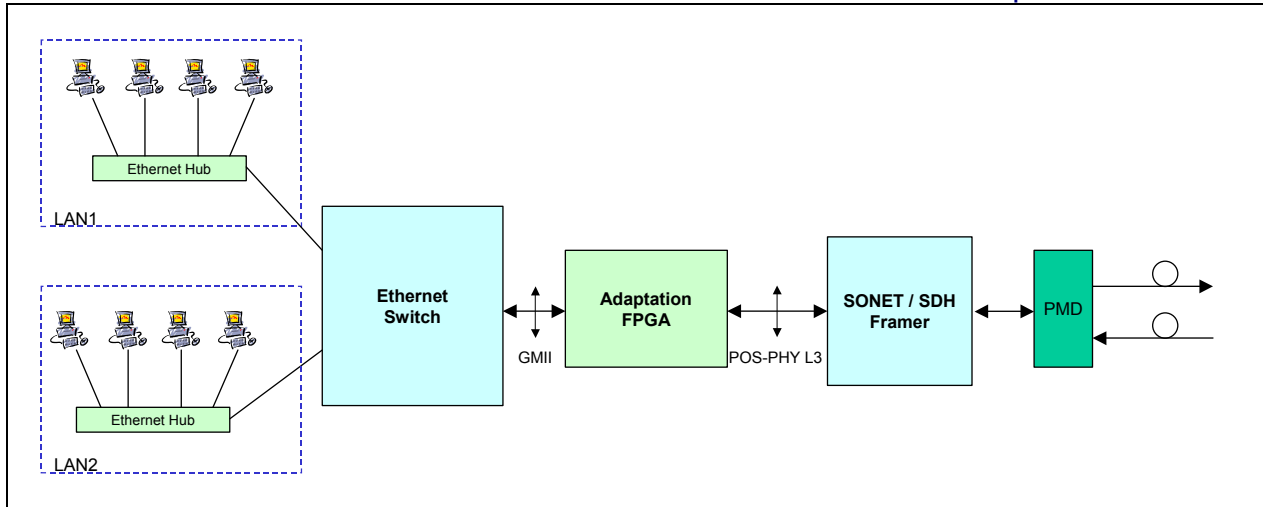


Figure 2: POS Application Example

The MorethanIP Ethernet switching solution provides a flexible and unique solution allowing designers to implement any additional function (e.g. PCI interface, POS-PHY / SPI packet interfaces,...) to complement the Ethernet switch and to provide connectivity to a large number of standard parts (e.g. SONET / SDH framers, VoIP processor) or systems (e.g. Proprietary backplane, host computer via PCI / PCI-X) with a single chip solution.

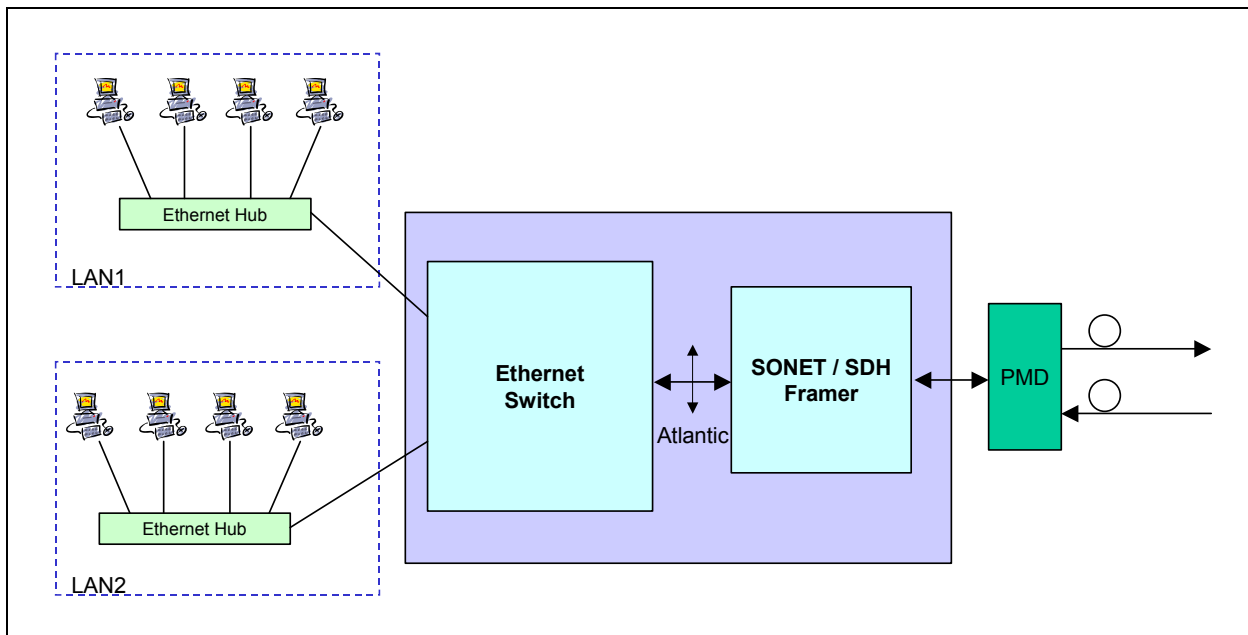


Figure 3: POS Application Example with MorethanIP Switching Solution

The MorethanIP switch implement a programmable number of Atlantic ports, which can be seamlessly connected to any Telecom Core from MorethanIP or to any third party Core supporting the Atlantic SOC (System on a Chip) standard. Each Atlantic port is 32-Bit wide.

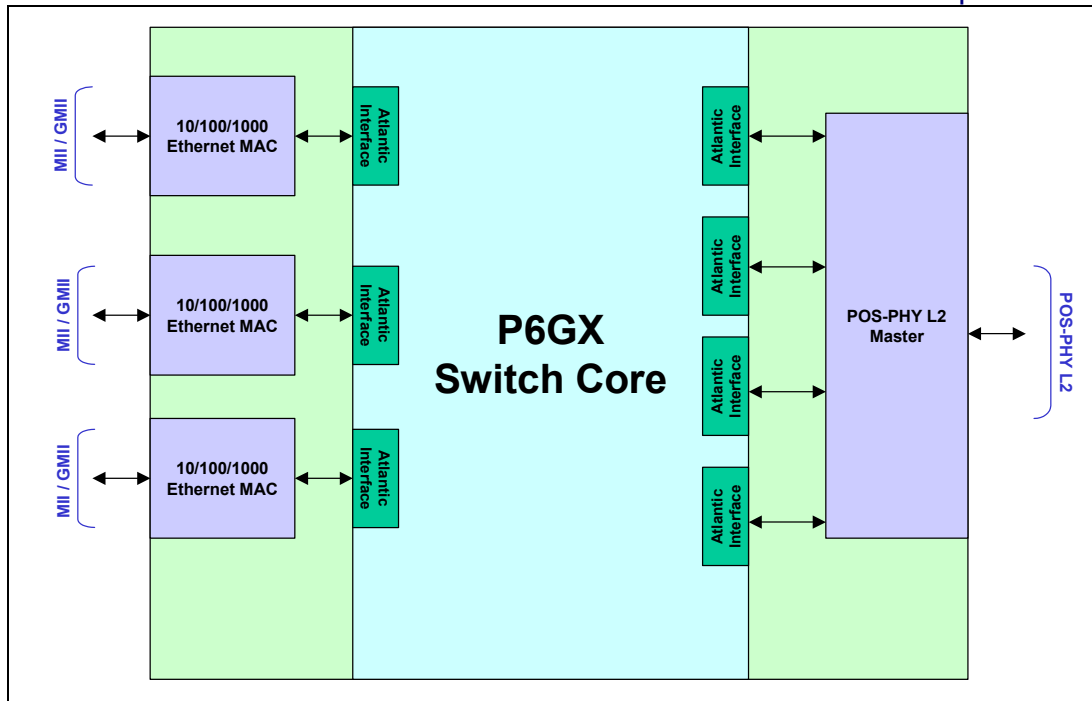


Figure 4: Integrated Switch Solution Example

In addition, standard Ethernet switches typically implement a large number of ports (12, 24) and implement a fixed distribution of ports (e.g. eight 10/100 Ethernet ports + 1 Gigabit Ethernet port) and therefore can provide an oversized or not adapted solution for applications that require only a few ports or a different repartition of ports.

The MorethanIP P6GQSX programmable switch provides up to 6Gbps-switching capability, which can be used as required by the User application. MorethanIP switch is implemented as a System on Chip (SOC) and it embeds a Hardware switch engine, for performance, and a 32-Bit processor, which performs learning, ageing, migration tasks and which can be programmed to implement any other high function such as Spanning Tree or any user specific task.

The MorethanIP P6GQSX Core is available on Altera Stratix FPGAs (Field Programmable Gate Array), which provides a quick time-to-market. The Switch Core can be migrated to Altera Hardcopy or ASIC devices to reduce costs.

2 P6GQSX 6Gbps Ethernet Switch Features

- Integrated Ethernet Switch engine with programmable number of SOC (System on Chip) ports (up to 15) seamless compatible with MorethanIP 10/100/1000 MAC Core
- 32-bit switching engine operating at frequencies up to 200MHz (+) on Altera Stratix-II FPGA providing 6 Gbps (+) non-blocking switching capacity
- Implements hardware switching look-up mechanism providing a learning capacity of up to 2K MAC addresses
- Switching table range can be reduced or enlarged, for optimized Firmware operation
- QoS Support with frame priority classification for flexible output queue management
- Optional Classification and Priority assignment based on Port Number, MAC Address, Ipv4 DiffServ Code Point Field, Ipv6 Class of Service and VLAN Priority (IEEE802.1q)
- Support Ethernet Multicast, Broadcast with flooding control to avoid unnecessary duplication of frames
- Programmable Multicast destination port mask to restrict frame duplication for individual multicast addresses
- Multicast and Broadcast resolution with VLAN domain filtering providing a strict separation of up to 32 VLANs
- Supports VLAN frames reception and transmission
- Programmable Ingress and Egress VLAN tag addition, removal and manipulation supporting single and double-tagged VLAN frames
- Supports configurable VLAN switching when MAC address lookup should be omitted
- Programmable number of IP Core interconnect Atlantic ports which can be connected to up to 15 Ethernet MACs, packet interface queues or custom logic
- Event and status signals which can be used to monitor port activity, severe error conditions or any user specific event
- Can be used in managed implementations with bridge protocol frame support (e.g. Spanning Tree protocols) or unmanaged implementations
- Generic processor interfaces which are typically connected to an embedded 32-Bit processor with 64K-Byte internal program memory sufficient for MorethanIP standard switching firmware (Learning, Aging, Migration and look-up management) and user specific tasks
- Processor Interface integration in Altera SOPC Builder when using Nios-II embedded processor as switch control processor subsystem
- Programmable firmware operation with Static or Dynamic (Learning, Aging) switching tables
- Switch firmware source available to provide customer specific software development capability
- Optional Spanning Tree Support
- Modular concept to allow for flexible output queue management implementations
- Available on Altera FPGAs, Altera Hardcopy devices or ASIC

3 Block Diagram

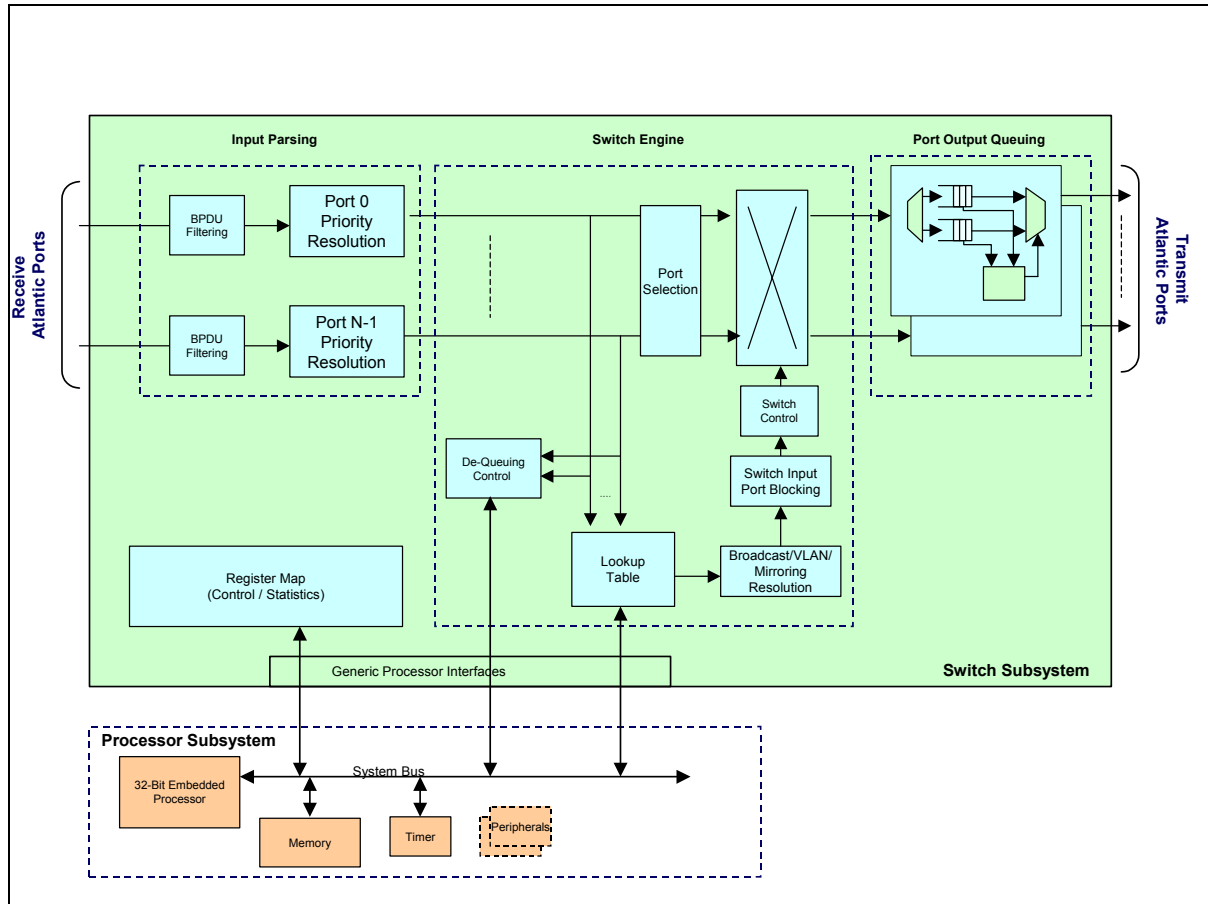


Figure 5: P6QSX L2 Switch Block Diagram

4 Implementation Summary

Table 1: P6QSX L2 Switch Complexity Summary

Device Family	Speed Grade	Complexity <i>(preliminary)</i>		Performances	
		L2 Engine	L2 Engine with Embedded NIOS Processor	Maximum Clock Frequency	Switching Capacity
STRATIX II	-5	6000 LEs ⁽¹⁾	8000 LEs ⁽¹⁾		6Gbps
	-3				8Gbps
STRATIX	-7	6000 LEs	8000 LEs		5Gbps
	-5				6Gbps

1. The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

5 Design Kit Overview

Table 2: Design Kit Overview

<i>Design and Simulation</i>	
Language	Source Code VHDL/Verilog, Encrypted VHDL or Verilog Netlist
Simulation	Configurable VHDL / Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive test environment with Ethernet frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
<i>Supported Design Tools</i>	
Simulation	Modelsim Version 5.7a or higher.
Synthesis	Quartus II 5.1 or higher
Implementation	Quartus II 5.1 or higher
Nios-II	V5.1 or higher

6 Contact

MorethanIP GmbH

Muenchner Str. 199

85757 Karlsfeld

Germany

Tel : +49 (0) 81313339390

FAX : +49 (0) 81313339391

E-Mail : info@morethanip.com

Internet : www.morethanip.com