Reference Guide
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PHYWORX

10/100/1000 Ethernet PHY Daughter Board

Reference Guide

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1 Introduction

The MorethanIP PHYWORX 10/100/1000 Ethernet PHY daughter board gives designers the ability to implement high-speed Ethernet solutions for prototyping and evaluation and embedded software development. The daughter board is designed for use together with development kit main boards like the Altera Nios Development Boards (Stratix and Cyclone editions). The daughter board provides Ethernet connectivity for speeds from 10Mbit/s to high performance Gigabit/s and interfaces directly to copper infrastructure (10/100/1000 Base-T) through a standard RJ45 connector.

In combination with MorethanIP 10/100/1000 Ethernet MAC the PHY daughter board allows to implement, prototype and test embedded Ethernet applications from 10 Mbps to Gigabit speeds with the same hardware and software environment. The PHY daughter board comes with software drivers and a TCP/IP reference implementation to allow for software development.

Figure 1: Daughter Board Top View

2 Features

The PHYWORKX Ethernet Development Kit includes the following components:

- High Performance Triple-Speed Marvell 88E1111 10/100/1000 Ethernet PHY
  - Autonegotiation for automatic speed selection
  - Automatic cable crossover configuration
  - Flexible Interface Support
    - Combined MII/GMII
    - RGMII
  - PHY Management Interface (MDIO/MDC) for configuration/status
- Standard Ethernet Copper RJ45 connector (10/100/1000 Base-T)
- Status LEDs for current speed and traffic indications
- Mechanically and electrically compatible with 74-pin Expansion Prototype Connector (Santa Cruz) for use with Altera Development Kit Mainboards
- Nios-II Reference design (FPGA programming files) with Ethernet MAC for immediate use of the PHYWORKX with Altera Nios-II Development Kit Mainboards.
  - 32-Bit Nios-II Processor with Peripherals and DMA
  - MorethanIP 10/100/1000 Ethernet MAC with Avalon Bus Interface
- C-Software drivers for TCP/IP protocol stack
  - Raw packet driver transmit and receive usage examples
  - Software Development Kit for the embedded System allowing software development for the embedded processor reference system.

3 Board Components Description

The PHYWORX Daughter Board contains a triple-speed Ethernet PHY device, magnetics and a standard RJ45 connector allowing connection to 10/100/1000 Base T networks. In addition, several status LEDs indicate the currently active mode of operation.

The triple-speed PHY device is configured to automatically select the operating speed when a network cable is plugged into the RJ45 connector using standard Autonegotiation to find out the remote partner and link capabilities. In addition to speed negotiation, the PHY automatically detects if crossover cabling is necessary or not.

The PHY can be programmed through the Managment Interface (MDIO) to change speed or enable serial loopback or to perform reset and autonegotiation functions during operation. The MDIO management address of the PHY is 18.

The PHYWORX daughter board is compatible to the 74-pin Expansion Headers as found on the Altera Nios Development Kits or similar main boards and is powered by the main board through a single 3.3V power rail. The connectors provide all signals implementing a combined MII (10/100 Mbps) / GMII (1000 Mbps) interface to the Main Board.

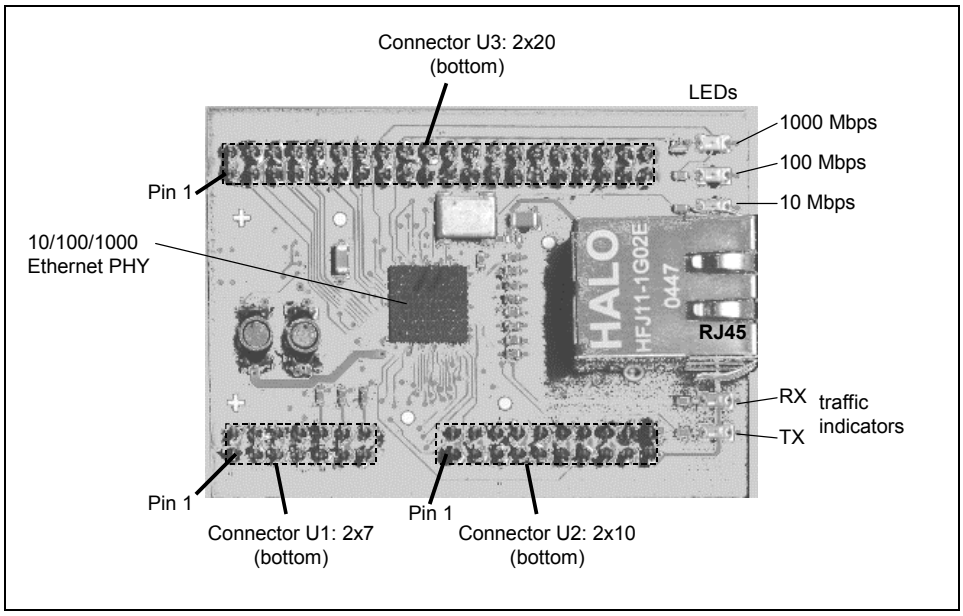

Figure 2: Daughter Board Components

3.1 Pins and Signals

Table 1: Connector U1 (2x7), Signals Description

Connector U1 Pin	Direction Daughter Board	Pin Name	Description
10	inout	mdio	Serial Management Data Input/Output
12	in	mdc	Serial Management Clock driven by MAC to the PHY. The PHY has a hard-wired MDIO address of 2.
14	out	phy_intr	Interrupt pin from the PHY. Configurable through PHY

			management registers.
1		GND	Ground Plane

Table 2: Connector U2 (2x10), Signals Description

Connector U2 Pin	Direction Daughter Board	Pin Name	Description
11	in	gtx_clk	125 MHz clock driven by the MAC when Gigabit Mode is active.
13	out	m_rx_clk	2.5 MHz / 25MHz / 125 MHz clock driven by PHY depending on current speed of 10 Mbps, 100 Mbps or 1000 Mbps respectively.
2,4,6,8,10,12,14,16,18,20		GND	Ground Plane
5,7	in	3.3V Vcc	3,3 V Power Plane, typ. 400 mA

Table 3: Connector U3 (2x20) Signals Description

Connector U3 Pin	Direction Daughter Board	Pin Name	Description
16	out	m_rx_col	Receive Collision Indication from PHY
13	out	m_rx_crs	Receive Carrier Sense Indication from PHY
3	out	gm_rx_d[0]	MII / GMII Receive Data 0 from PHY
6	out	gm_rx_d[1]	MII / GMII Receive Data 1 from PHY
5	out	gm_rx_d[2]	MII / GMII Receive Data 2 from PHY
8	out	gm_rx_d[3]	MII / GMII Receive Data 3 from PHY
7	out	gm_rx_d[4]	GMII Receive Data 4 from PHY
10	out	gm_rx_d[5]	GMII Receive Data 5 from PHY
9	out	gm_rx_d[6]	GMII Receive Data 6 from PHY
12	out	gm_rx_d[7]	GMII Receive Data 7 from PHY
14	out	gm_rx_dv	MII / GMII Receive data valid indication
11	out	gm_rx_err	MII / GMII Receive data error
4	out	m_tx_clk	2.5 MHz / 25 MHz Transmit Clock driven by PHY when 10 Mbps / 100 Mbps speed is active. No clock is driven when Gigabit speed is active.

31	in	gm_tx_d[0]	MII / GMII Transmit Data 0 to PHY
29	in	gm_tx_d[1]	MII / GMII Transmit Data 1 to PHY
28	in	gm_tx_d[2]	MII / GMII Transmit Data 2 to PHY
27	in	gm_tx_d[3]	MII / GMII Transmit Data 3 to PHY
25	in	gm_tx_d[4]	GMII Transmit Data 4 to PHY
23	in	gm_tx_d[5]	GMII Transmit Data 5 to PHY
21	in	gm_tx_d[6]	GMII Transmit Data 6 to PHY
18	in	gm_tx_d[7]	GMII Transmit Data 7 to PHY
15	in	gm_tx_en	MII / GMII Transmit enable
17	in	gm_tx_err	MII / GMII Transmit error
1	in	reset_n	Reset input (active low) to the PHY.
2,22,24,26,30,34,40		GND	Ground Plane

4 FPGA Pinouts for Selected Main-Boards

The PHYWORX daughter board connects directly to Altera Main-Boards that provide the 74-pin Prototype Expansion Header ("Santa Cruz"). The following table lists the pinout for the daughter board connector wired to the FPGA of the Main Board chosen.

Table 4: Main-Board FPGA Pinouts

Pin Name	Direction (FPGA)	Cyclone 1C20 F400 (Nios Dev. Kit)	Stratix 1S10 Stratix 1S40 F780 (Nios Dev. Kit)	Stratix 1S40 F1020 (High-Speed Stratix GX-Dev. Kit)	Stratix-II (Nios Dev.Kit)	Cyclone-II (Nios Dev.Kit)
Connector Name:		"PROTO2" J15, J16, J17	"PROTO2" J15, J16, J17	"Santa Cruz"	"Proto2" J15,J16,J17	"Proto2" J15,J16,J17
gtx_clk	out	(=PLD_CLK OUT:L8)[1]	(=PLD_CLK OUT:E15)[2]	AL18	A12	F20
m_rx_clk	in	K14	R4	B15	B14	AF14
m_rx_col	in	W13	AH22	A9	J17	V18
m_rx_crs	in	R14	AD21	B9	C18	AD21
gm_rx_d[0]	in	T15	AD19	A11	H15	AE24
gm_rx_d[1]	in	U15	AH20	C13	A17	AF23
gm_rx_d[2]	in	Y15	AF18	C12	C16	V22
gm_rx_d[3]	in	V14	AF20	E13	A18	AC22
gm_rx_d[4]	in	V15	AH21	D13	C17	AE23
gm_rx_d[5]	in	Y14	AF21	B13	K16	AD23
gm_rx_d[6]	in	U14	AE20	A13	F17	AB21
gm_rx_d[7]	in	T14	AE21	E11	A19	AC21
gm_rx_dv	in	V13	AG20	D10	C19	AF22
gm_rx_err	in	W14	AG21	D12	G17	AD22
m_tx_clk	in	W15	AE19	B12	J15	T21
gm_tx_d[0]	out	Y12	AE24	A8	B22	AE20
gm_tx_d[1]	out	W12	AH24	E9	C22	AF20
gm_tx_d[2]	out	T11	AE23	B8	D18	AC20
gm_tx_d[3]	out	T12	AG23	D8	J18	AB20
gm_tx_d[4]	out	U12	AD23	B7	E18	AE21
gm_tx_d[5]	out	V12	AF23	D11	A22	AF21
gm_tx_d[6]	out	T13	AH23	B10	C21	U18
gm_tx_d[7]	out	R13	AE22	C11	C20	U17
gm_tx_en	out	U13	AG22	C10	A20	AE22
gm_tx_err	out	Y13	AF22	B11	A21	W19
mdio	inout	Y10	W18	E7	B17	AA16
mdc	out	U11	Y17	C3	B19	AC17
phy_intr	in	Y11	AB19	C4	G18	AF17

Notes:

1) On the Nios Development Kit, Cyclone Edition, the 125 MHz transmit clock to the PHY is driven by the dedicated PLL clock output named "PLD_CLKOUT", FPGA Pin L8. The clock is generated by the internal PLL multiplying the 50 MHz oscillator input clock by 5/2.

2) On the Nios Development Kit, Stratix Edition, the 125 MHz transmit clock to the PHY is driven by the dedicated PLL clock output named "PLD_CLKOUT", FPGA Pin E15. The clock is generated by the internal PLL multiplying the 50 MHz oscillator input clock by 5/2. This also leads (due to board layout constraints) to the SDRAM clock being driven with 125 MHz, which therefore is not usable with the standard Nios SDRAM controller and should be deactivated (CKE low, CS high)

5 MDIO Registers

The PHY provides 32 internal management registers that can be accessed using the Management Interface (MDIO). The Management Device Address of the PHY is configured to the value 18 (0x12).

See also IEEE 802.3 Clause 22.2.4 for details on the Management Register Bits.

Table 5: MDIO Registers Description

Register	*Name*	*Description (Bits)*	*Type*	*Reset Value*
0	Control	15: 1=PHY Reset, 0=normal operation. (SC) 14: Loopback. 1=enable loopback, 0=normal operation 13: Speed Selection (together with Bit 6): 6:13 = "11": reserved = "10": 1000 = "01": 100 = "00": 10 12: Enable Auto-Negotiation (only enables the control state machine, does not trigger the auto negotiation). If disabled (0), bits 6,8,13 define the operation. 11: Power down (1) or normal operation (0) 10: Isolate PHY from GMII/MII (if 1) 9: Restart Autonegotiation. If set (1) will restart the autonegotiation process. 8: set full duplex mode (1) or half-duplex (0) 7: Enable collision test signal (1) 6: Speed Selection (see Bit 13 above). 5:0 reserved. Write 0, ignore on read	RW	
1	Status	15: 100 Base-T4 support 14: 100 Base-X full-duplex support 13: 100 Base-X half-duplex support 12: 10 Mbps full-duplex support 11: 10 Mbps half-duplex support 10: 100 Base-T2 full-duplex support 9: 100 Base-T2 half-duplex support 8: Extended Status is available in register 15 if 1 7: reserved. Ignore on read 6: PHY accepts MDIO preamble suppression (1) 5: Auto Negotiation Complete (if set) 4: remote fault condition detected (1) 3: PHY is able to perform Auto-Negotiation (1) 2: Link Status Latch: Indicates if link was good (1) since last status read or link was lost (0) since last status read 1: jabber detect 0: Extended Register capabilities are available (1)	RO	

Register	*Name*	*Description (Bits)*	*Type*	*Reset Value*
2	PHY ID1	Bits 31:16 of PHY identifier	RO	0x0141
3	PHY ID2	Bits 15:0 of PHY Identifier (bits 3:0 = revision)	RO	0x0cc2
4	Adv	Autonegotiation Advertisement Register 15: Next Page Transfer desired 14: reserved 13: Advertise remote fault 12: reserved 11: MAC supports asymmetric Pause 10: MAC supports Pause frames 9: 100Base-T4 support (always 0) 8: 100Base-TX full duplex support 7: 100Base-TX half duplex support 6: 10Base-T full duplex support 5: 10Base-T half duplex support 4..0: support for IEEE 802.3 ("00001")	RW	
5	RemAdv	Autonegotiation Link Partner Ability Register	RW	
6	ANER	Auto-Negotiation Expansion 15..5: reserved 4: Fault has been detected via parallel detection 3: Link Partner does support next page (1) or not (0) 2: Local device supports next page 1: Link Code word received. Cleared upon read. 0: Link Partner supports Auto-Negotiation	RW	
7	ANNPTR	Auto-Negotiation Next Page Transmit	RW	
8	ANNPRR	Auto-Negotiation Link Partner received Next Page	RO	
9	1KTCR	1000 Base-T Master-Slave Control Register 15..13: test modes. "000" normal operation 12: enable manual master/slave configuration 11: Set PHY as Master (1) or Slave (0) if Bit 12=1 10: Advertise device as Multi-Port (1) or Single-Port (0) 9: Advertise 1000 Base-T fullduplex capable 8: Advertise 1000 Base-T halfduplex capable 7..0: reserved	RW	
10	1KSTSR	1000 Base-T Master-Slave Status Register 15: Master/Slave manual configuration fault detected 14: Configuration resoved to Master (1) or Slave (0) 13: Local receiver Status Ok (1) or not (0) 12: Remote receiver Status Ok (1) or not (0) 11: Link Partner fullduplex capable 10: Link Partner halfduplex capable 9..8: reserved 7..0: IDLE error count	RO	
11		reserved		
12		reserved		

Register	*Name*	*Description (Bits)*	*Type*	*Reset Value*
13		reserved		
14		reserved		
15	1KSCR	Extended Status 15: fullduplex 1000 Base-X supported 14: halfduplex 1000 Base-X supported 13: fullduplex 1000 Base-T supported 12: halfduplex 1000 Base-T supported 11..0: reserved	RO	
Vendor Specific Registers				
16..31		vendor specific		

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